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HIGH EFFICIENCY MICROWAVE POWER AMPLIFIER DESIGN

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High efficiency microwave power amplifier design

by

Edward William Harriott

A Dissertation Submitted to the

Graduate Faculty in Partial Fulfillment of the

Requirements for the Degree of

DOCTOR OF PHILOSOPHY

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1. INTRODUCTION

1.1. Introduction

Over the last ten years, microwave semiconductor device technology has progressed rapidly. Gallium arsenide field-effect transistors (GaAs FET), silicon bipolar transistors, IMPATT, Gunn diodes and Tunnel diodes are now widely used in solid-state amplifiers for communication systems. From uhf to 4 GHz, silicon bipolar transistors are dominant in performance in low noise, high gain, and high power amplifier applications. The current revolution in the amplifier area started with the GaAs FET, which is capable of providing low noise, high gain, power amplification from 2-20 GHz. Octave bandwidth GaAs FET amplifiers within this frequency range have been built, and research in the millimeter wave region will probably provide FETs capable of performance at frequencies up to 40 GHz. The IMPATT diode provides higher power amplification of up to 100 GHz, particularly in pulse power amplifiers. An excellent chronological review of this growth and development is provided within the listed references [1-15].

Even though the GaAs FET has a lower noise figure, a higher gain, and higher power capability at frequencies above 4 GHz, the bipolar transistor still dominates in the lower frequency range. Silicon is the preferred semiconductor for microwave bipolar transistors.

1.2. Microwave Bipolar Transistor Fabrication

Microwave bipolar fabrication technology is basically the same as that of lower frequency transistors, except that attention must be directed towards the factors that limit the frequency performance, such as the emitter width, the emitter-to-base contact spacing and the collector

area. The maximum oscillation frequency is inversely proportional to the emitter width and emitter-to-base spacing. Most microwave silicon bipolar transistors use the planar process and all are n-p-n. The critical device dimensions are etched into layers of SiO_2. These etched patterns are called the geometry of the transistor.

The process begins on an n-type epitaxially grown silicon layer that has resistivity in the range from 0.5 to 2 Ω/cm. The epitaxial layer is 2 to 5 μ thick and is supported by a heavily doped n^+ substrate which forms the collector contact. A thermally grown oxide layer of approximately 0.5 μ is then formed on the surface of the n-layer. Using photo-resistant exposure, window openings are produced and etched to allow a p^+ diffusion for the base area. Through the open window, a heavily doped p-type diffusion is made to provide low resistance contacts to the base region. The base area is then cut into the oxide. A lightly doped p-type diffusion is performed through the base opening and then connected to the p^+ region. An additional SiO_2 deposition on the base area is also provided for emitter masking. Windows are then opened in the base oxide to form emitter contacts. The process is completed by diffusing a shallow, heavily doped, n-type layer into the emitter opening. The contact metallization, which may be either aluminum based or gold based, is deposited and the contact pattern is defined and etched. Ohmic contacts are obtained by sintering at about 425°C. This process is called "diffused planar" technology [16].

1.3. The Bipolar Microwave Power Amplifier

Power amplification employed in transmitting systems requires the amplification of high-level signals to furnish considerable signal power to a load such as an antenna. The amplifiers used for these purposes are called power amplifiers or large-signal amplifiers. They are biased at a high current level; therefore, their efficiency is of major importance. Because of the large input signal level, the transistor parameters now vary appreciably over the signal cycle, thus resulting in output signal distortion. For these amplifiers, small-signal S-parameters are of limited value for the design of matching networks. The large-signal S-parameters are ill-defined and are not often available. Therefore, large-signal input and output impedance values are typically obtained by using the conventional substitution methods.

The power amplifier input signal level is high. Consequently, the collector current is either in the cutoff or saturation region during a portion of the input signal cycle. This leads to the classification of power amplifiers into three basic modes of operation: Class-A, Class-B, and Class-C. In the Class-A amplifier mode, the collector current flows for 360° of the input voltage cycle. The Class-B amplifier limits the collector current flow to 180° of the input voltage cycle and the amplifier is biased at cutoff. Class-C amplification collector current flow is less than 180° of the input voltage cycle and the amplifier is biased beyond cutoff [17-22].

Other amplifier identifications such as Classes D, E, F, G, H, and S may all be related back to one of the three basic classifications defined by the output current conduction angle and bias [22]. Using other

than a sinusoidal input signal source, the unique feature identifying each of the different amplifier types is related to either input or output signal wave-form control. The various device properties required to attain the desired performance place large restrictions upon both frequency and bandwidth capabilities. In all of these specifically defined operating modes, improved dc to RF conversion efficiency is the primary objective. However, as with the basic Class-C mode, the theoretical unlimited efficiency improvement is accompanied by reduced power output capability. The trade-offs do not always require a reduced power output as a compromise for improved efficiency. Other operational parameter limitations related to both the device maximum ratings and the output signal bandwidth impose equally compromising, but different limitations.

1.4. Dissertation Objectives

The above discussion provides a generalized view of both the evolutionary growth of microwave devices and the microwave power amplifier.

Solid state microwave amplifier design is a dynamic and rapidly growing field. Its principles are well-formulated. Many aspects of amplifier design stem from vacuum tube technology. The purpose of this dissertation is to define a technique that can be applied to new solid-state devices.

The approach shall be to use the most common amplifier configuration the "Zero Biased Microwave Power Amplifier," and to define its operation. The operational definition shall emphasize the calculation of the collector output load impedance and the dc to RF conversion efficiency.

Through this development, a functional model applicable for design use will be defined. The completed model will be evaluated and compared to actual measured transistor performance parameters.

The use of the model design concept and the described test procedure provides a quick and accurate method to obtain design data for initial designs and computer aided design (CAD) applications.

2. REVIEW OF PRIOR RESEARCH

2.1. Introduction

The operating characteristics of large-signal devices are a function of both the signal level and the circuit impedance. Most designs have been based upon "cut and try" designs using manufacturer's provided test data or empirical designs [23, 24].

2.2. RF Amplifier Design

Much of the published RF amplifier design research has been directed toward the ideal transistor. Both the theoretical analysis and the experimental test results have been used to describe and characterize the operating dynamics. The ideal transistor concept is preserved by conducting the experimental work at very low frequencies and power levels. At low frequencies and power output levels the non-linear characteristics of the transistor are reduced and/or eliminated, resulting in near ideal device performance [25-33].

Non-linear analysis of large-signal, high power amplifiers utilizing complex non-linear models has been developed using the large-signal Ebers-Moll equations [34]. Both the collector efficiency and the power gain can be calculated as closed functions of input level. The results are obtained without recourse to graphical methods or to piecewise-linear approximations [25,26]. The major limitations are the ideal transistor approximations used to avoid the high current and the frequency effects that are more pronounced at the upper operating limits. The models are represented mathematically in terms of non-linear differential equations. The solution of the equations requires transient analysis, which is

practical only with the aid of a digital computer using programs such as Net-1, SCEPTRE, or CIRCUS.

Transistor characterization by effective large-signal parameters measured under the condition of sinusodial excitation using two-port immittance scattering parameters is an alternative method for active-device description [35-37]. This method loses its appeal because of the large amount of measured data required for even limited ranges of frequency and bias. A further drawback is its conventional restriction to the linear operating domain.

Often applied to interface varactor multipliers to transistor power stages, load-pull characterization methods are also used to characterize large-signal transistor output impedances [38-40]. Conceptually, this method is an extension of the technique of tuning the transistor to a specific operating condition such as power input, power output, collector current, etc., then removing the impedance matching networks, and then using a network analyzer system to characterize the load network. By using a large number of measured data, constant-power output, constant-current, constant-gain, etc., loci are then plotted on Smith charts. From these plotted data, optimum load impedance terminations for the amplifier are selected.

Load-pull characterization is currently considered to be the most elaborate technique for transistor output characterization. However, there are limitations and disadvantages to this method. When using manual measurement techniques, the primary objective of maintaining a condition of constant output power, collector current or power gain over an output load impedance range large enough to produce a closed contour on a Smith

chart, is a time consuming task. This characterization at several different frequencies for broadband design applications, can consume a prohibitive amount of time. An automatic impedance-tuning apparatus, coupled with a self-optimizing search algorithm, can eliminate the burden of the required effort, but may not be an economically feasible solution. If extreme care is not taken during the measurement procedure, large measurement error may result. After the established operating conditions have been attained, measurement error susceptibility arises from the necessity of transferring the tuned load-matching networks to the network analyzer system for independent measurement [41].

2.3. Transistor Modeling

Transistor models have been developed and used to facilitate optimization of a transistor design and performance. The degree of complexity of a transistor model is always a compromise between the accuracy of the transistor representation and the ease of application and analysis. Traditionally, comparatively simple models have been used to characterize high-frequency, small-signal transistors. However, at large-signal levels these simple models fail to provide adequate results due to the non-linear effects prevalent under large-signal conditions. These effects are typically the result of internal parasitics and non-linear mechanisms within the transistor which generate harmonic voltage and current components.

High-power, high frequency transistors are classically modeled by the hybrid-Pi model [42]. This model is the most popular high frequency equivalent circuit for a junction transistor. The parasitic

lead inductances of the packaged device are defined constants. The remaining parameters represent the intrinsic transistor. Although each of the parameters varies with the instantaneous signal level, and therefore time, they are normally assumed to have fixed values which are a function of the average level of operation. With judicious selection of parameter values, the model can be adjusted to predict small- and medium-signal performance over a wide frequency range. The model fails to characterize a transistor when it is driven into saturation. This is best understood by viewing the various operating regions of the transistor operation.

The transistor operation may be described by three operating regions:

1) In Region I, the off or cutoff region, only leakage currents flow because both the collector-base and emitter-base junctions are reverse biased.
2) In Region II, the active region, the collector-base junction is reverse-biased, and the emitter-base junction is forward-biased.
3) In Region III, the on region, both the collector and emitter base junctions are forward biased.

Because the hybrid-Pi model does not include a collector-base diode, it can accurately represent operation in the active and off regions, but not in the on region. However, a transistor operating under large-signal conditions is predominantly either on or off, and switches rapidly through the active region. As a consequence, the model fails to describe the heavily overdriven transistor. A much more complex model is required to define and characterize the saturated (on) region of operation.

The Linvill lumped model [43], the Beaufoy-Sparkes charge-control

model [31, 44-47], and the Ebers-Moll model [34] introduce a representative solution of the relations describing the distributed base region and the resulting intrinsic characteristics presented by the transistor.

The Linvill lumped model is defined by the solution of the continuity equation for current carriers at finite time intervals in the base. The solution provides a set of lumped element values which are treated as a network. The number of sections into which the base is subdivided determines the accuracy of the resultant device representation. This model provides the most accurate physical description of the transistor, but is unwieldy to analyze.

The Beaufoy-Sparkes charge-control model focuses upon the relationship between the terminal currents and the minority-carrier stored charge. The resulting equations which describe this relationship are then modeled by circuit elements. Circuit analysis of the resulting model provides the transistor representation.

The Ebers-Moll model is based upon the concept of superimposing normal and inverse transistors in which the collector-base and emitter-base junctions are modeled as capacitor shunted diodes. The major deficiency of this model is that it does not account for the effects of carrier storage. Carrier storage effects are dominant at the upper frequency limits.

The described models have been selectively used to represent and describe the internal parameter of both large and small signal operating conditions of transistors. Examples of the model applications are developed in the cited references [48-51].

2.4. Large-Signal Transistor Intrinsic Effects

Microwave transistors operating at large-signal levels (power amplifiers) may be subject to operating conditions which produce highly non-linear effects. These non-linear effects result from the intrinsic internal parasitic elements inherent to the transistor.

The two major effects which predominate in microwave power amplifier performance relate to the effective collector-to-base capacitance value and the RF emitter saturation voltage V_{sat}.

The collector-to-base capacitance non-linearity results from the base widening effects (Kirk effect), which in turn reduces f_t at high collector current densities [52-55]. The current-dependent buildup of the mobile-carrier space-charge density in the collector transition layer at high collector current levels results in space-charge densities that are comparable to the fixed charge density of the collector transition region. The resulting effect is the displacement of the transition boundary adjacent to the neutral base layer towards the collector contact pad. This widening of the neutral base layer increases the effective collector-to-base capacitance (C_{ob}). The increase of C_{ob} reduces f_t. This, in turn, reduces the operating efficiency resulting in increased power dissipation. The increased power dissipation elevates the operating temperature.

While the Kirk effect predominates at the high collector voltage and current operating conditions of large-signal operation, the effects of emitter saturation [56] are experienced as a predominant factor at low collector voltages and high collector current. The resultant amplifier degradation is effectively the same: reduced efficiency and

power output, with the associated runaway thermal effects produced by the increased power dissipation.

2.5. RF Transistor Design Compromises

The goemetric design of microwave transistors is a primary factor in determining reliability and RF performance which ultimately contributes to the physical elements defining the current distribution and densities. The effective collector parasitics, lead parasitics, and package capacitances are related to the physical geometry of the transistor design [57-61].

At microwave frequencies, the injected currents flow near the edge of the emitter sites. The current-handling level must be translated into an emitter-periphery ratio requirement. This requirement is definable only if the current-handling capability per mil of emitter periphery is known. Typically, these periphery values range from 1 to 1.5 milliamperes per mil. The emitter periphery (EP) is defined as:

$$EP = \frac{I_c}{I_{m/\ell}}$$

where:

EP = emitter periphery (mils)

$I_{m/\ell}$ = the maximum collector current per mil of EP in mA/mil, and

I_c = the collector current in milliamperes.

While using the minimum emitter area to optimize the frequency response capability of an RF transistor, it is essential to package the required EP into the smallest practicable base area. The minimum

emitter area (EA) is required to reduce the input capacitance to minimize the shunting of the emitter-base diode. This input junction capacitive reactance decreases with increasing frequency, resulting in reduced base current injection.

Output current shunting is similar to the input current shunting described above. The load current is reduced by the collector-to-base effective capacitance which is closely related to C_{ob}. The major degree of freedom available to minimize C_{ob} capacitance effects is to increase the collector resistance. Increased collector resistance promotes base widening and limits the power output level. The resultant design must optimize the emitter periphery to base area ratio, EP/BA.

In addition to optimizing both the EP/EA and EP/BA ratio within the limits of the available technology, other geometric factors must be considered. These include thermal resistance, current distribution, current densities in the metalized fingers, adaptability to emitter ballasting and reduction of parasitic capacitances and inductances.

2.6. Summary

The review of prior research has provided a broad survey of the most current research related to microwave power amplifier design and is not in any way intended to be all-inclusive. This survey serves to illustrate both the large range of research diversity and depth of investigation in this specific area.

Technological limitations of both fabrication and measurement instrumentation have been described. Many theoretically constructed models have been developed to describe and emphasize the specific

physics-related intrinsic phenomena of the transistor. The basic amplifier operational modes using the ideal transistor have been mathematically modeled. Definitions and associated mathematical relationships have been formulated to describe the functional performance for both measured and calculated data. However, more research and development remains to be done in order to direct the results of the diverse research towards design applications. There exists an urgent need for efficient, accurate microwave power amplifier design techniques.

Sections 3 and 4 discuss the design question, and provide a proposed and tested design approach.

3. ZERO BIASED MICROWAVE POWER AMPLIFIER DESIGN

3.1. Introduction

Extensive characterization and design procedures have been developed for transistors operating at small signal levels [48, 62, 63]. Similar research work conducted to characterize power amplifiers has not effectively provided a generalized design procedure. Many different analytical approaches have been employed to provide a theoretically valid performance analysis predicated upon controlled parameters such as conduction angle (θ), input current or voltage wave form control, collector wave form shapes, or harmonic frequency loading to identify a few. Most research work has been conducted at low frequency and power levels relative to the power and frequency capabilities of the device used to provide operating performance data [26, 45]. All of this work, though not directly applicable to design application, has helped to describe many important characteristics of the transistor operating dynamics [25, 26, 31, 45].

Microwave power amplifier designs generally require that the transistor function be at or near its maximum rated frequency and output power level. Other performance parameters such as operating bandwidth, power output gain, etc., add further to the design complexity. Design attempts to obtain maximization of amplifier operational performance immediately produce situations which violate the analytical and experimental conditions assumed in the support of prior low power and frequency amplifier research [25, 26, 31].

The final design, which is often described as an optimal design to

reflect the maximization of specifically desired performance characteristics, results in a best fit compromise of all the interacting parameters of the transistor.

Relative to the transistor development, little has been achieved in non-linear modeling of the device for circuit design. There are fundamentally two approaches to non-linear device modeling. Both are based upon the solid state physics approach and are frequently referred to as the device model and the device equivalent circuit model.

The device model approach is based upon the physical mechanisms that lead to the device operating characteristics. The physical mechanisms of the device are represented in terms of the basic partial differential equations, such as Poisson's equation and the diffusion equation, which govern the behavior of the charge carriers in the semiconductor material. These equations are solved numerically with boundary conditions applied at the electrical terminals. The essential input quantities are the doping concentration, the geometry, and the applied bias. The output quantities are the electric field, the carrier concentrations, and the current densities. From these, the terminal current and signal delay times, etc., are calculated. In principle, all linear and non-linear effects can be explicitly included and the device behavior can be calculated to a theoretically unlimited accuracy if desired. However, in practice, the device model approach has been limited to one dimension because of the prohibitively long computer time and large memory storage required to solve the basic equations in two and three dimensions.

The second approach, the device equivalent circuit model, uses lumped and distributed elements to approximate the various three dimensional

mechanisms associated with the device operation. Therefore, the physical device functions are not explicitly represented. Usually, because of the excessive computer time and memory space required, only a one-dimensional model is attempted. These models are composed of combinations of standard circuit elements and controlled sources. The equivalent circuit models are more suitable for computer modeling and simulation because of the relatively reduced complexity as compared to the device model.

In either case, these modeling approaches yield circuit models with a large number of elements. Many of the elements must be approximated using curve-fitting techniques of data obtained from other experimental results. The end result is a very complicated model [64-68]. A further disadvantage of these models is the extreme difficulty in formulating a systematic procedure that would apply to a large variety of devices.

An alternative modeling approach, which is used in this dissertation, is based upon viewing the transistor output as a current switched 2-port circuit. The frequency and power range were limited to allow piece-wise linear approximations to be used in the model. In contrast to the non-linear models which are based on physical principles related to the device design and fabrication process parameters, the validity of this proposed model shall be related to amplifier performance. The amplifier measured performance will be correlated back to the design model to substantiate the proposed modeling design.

3.2. Objectives

The major emphasis of this dissertation shall be the development of an amplifier design technique which will be oriented toward circuit

design applications. The proposed procedure shall include the implementation of a functionally oriented model developed to describe the device parameters from a circuit design viewpoint. Amplifier performance measurements shall be compared with the predicted performance defined by the transistor model. The relative comparison of the model predicted performance to the measured performance will clearly substantiate the validity of the approximations and assumptions used in the model development.

The use of currently available Computer Aided Design programs (CAD) provides excellent design support for final design optimization. However, the CAD program results are dependent upon the accuracy of the input data. The required input data describe the transistor's parameter values assumed at specific operating conditions within the operating design range under consideration. Typically, these data are extrapolated from the manufacturer's supplied device data sheets or from the amplifier's performance measurements obtained using breadboard test circuits on the amplifier. Breadboard test circuit modeling is time consuming because of the amount of circuit modification and tuning required. In either case, the resultant data are seldom accurate enough to provide good first order design results. The advantages of an amplifier design model to provide CAD input data of good accuracy for rapid first order designs are obvious.

The purpose of this design procedure is threefold:

1) To establish a modeling technique which will permit the use of sinusoidal analysis approximations and to provide sufficient accuracy to be usable as a circuit design tool;

2) To define the conversion efficiency (η) along with the other important performance characteristics relative to the power output level, frequency, and dc supply; and
3) To demonstrate the validity of the applied technique with measured amplifier test data.

3.3. Model Definition

The proposed model should satisfy the following criteria:

1) It must be a simple, easily applied design modeling procedure;
2) It must provide reasonably accurate approximations of amplifier design parameters and performance characteristics; and
3) It must utilize direct linear analysis techniques.

Using the above criteria which are intended to describe a non-linear device such as a power transistor will result in a less than perfect model because of the approximations involved. The presently developed non-linear models require device information normally unavailable to the design engineer [25, 26, 42, 43].

Microwave power amplifier transistors are primarily of common base circuit configuration. Reasons for this are the enhanced power gain due to package parasitics, and reduced susceptibility to low frequency oscillation. The low frequency unilateral power gain of a common base design transistor is substantially lower than the same device mounted in a common emitter amplifier configuration [69].

The first step of the model development requires defining the common

base transistor configuration. Much work has been accomplished in the development of theoretical transistor modeling [26, 43]. Most of the developed model variations have been derived from the basic Ebers-Moll model [34] or the Gummel-Poon model [46]. The variations of these basic models provide an extremely broad selection [47]. The Tee model [43] provides a very direct and easily adapted basic configuration for development as shown

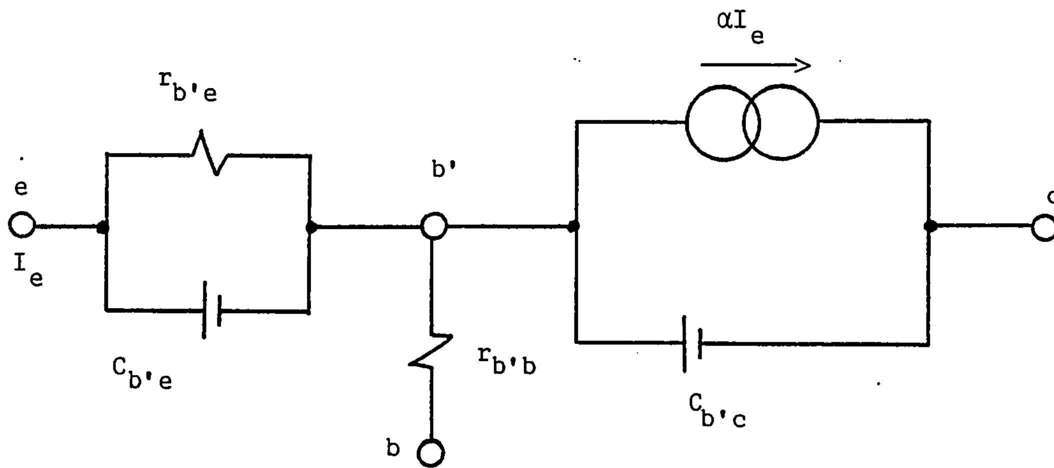


Figure 1. Tee model

where:

$r_{b'b}$ = base spreading resistance

$$r_{b'e} = \frac{1}{(1/r_{b'e}) + g_m} \approx \frac{1}{g_m}$$

g_m = transconductance

α = current gain $\equiv \frac{\alpha_o}{1 + j\omega/\omega\alpha}$

$C_{b'e}$ = base charging capacitance $\approx \frac{g_m}{\omega_t} - C_{b'c}$

$C_{b'c}$ = collector base depletion capacitance $\approx C_{ob}$

The model in Figure 1 must be further modified for microwave power transistor use. The resultant parallel impedance produced by $C_{b'e}$ in parallel with $r_{b'e}$ is very small when compared to the base spreading resistance ($r_{b'b}$) and, therefore, may be neglected in the model [43]. The addition of bond wires and distributed package parasitic inductances must be added to the emitter, base and collector elements. These modifications are described in Figure 2 below.

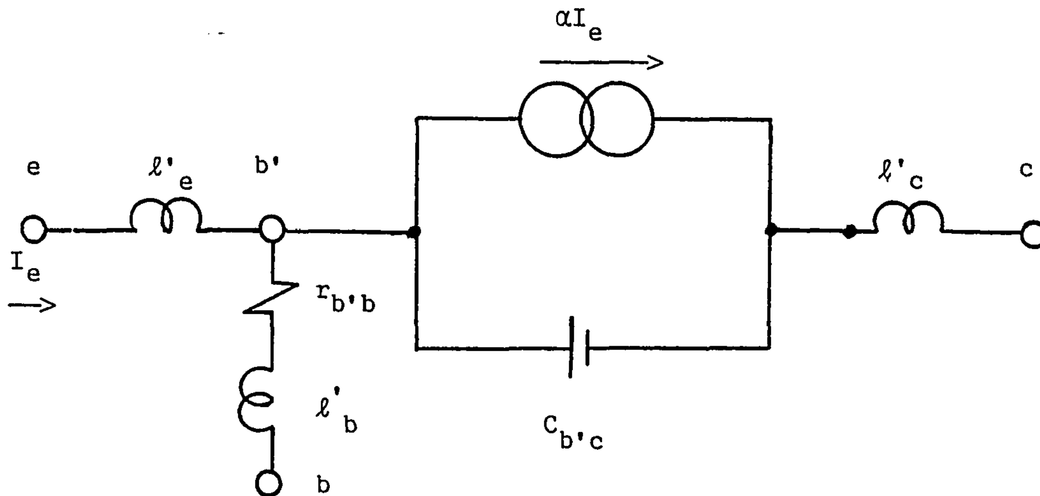


Figure 2. Modified Tee model

where:

ℓ'_e, ℓ'_b, and ℓ'_c represent the internal distributed parasitic and bond wire inductance of the emitter, base and collector elements respectively.

Further simplification is obtained by converting the model in Figure 2 into a unilateral equivalent circuit [43] shown in Figure 4. The separation of the model in Figure 2 to yield the unilateral equivalent circuit is based upon the assumption that the collector load reactance, combined with the sum of all the collector reactances, forms a resultant conjugate collector load equal to R_L, $(Z_L = R_L + jX_L)$, where $R_L > r_{b'b}$. The derivation of this procedure is illustrated by first changing the current source (αI_e) and the parallel capacitor $(C_{b'c})$ to a voltage source $\left(\frac{-j\alpha}{\omega C_{b'c}}\right)$ and a series capacitor $\left(\frac{-j}{\omega C_{b'c}}\right)$ as in Figure 3.

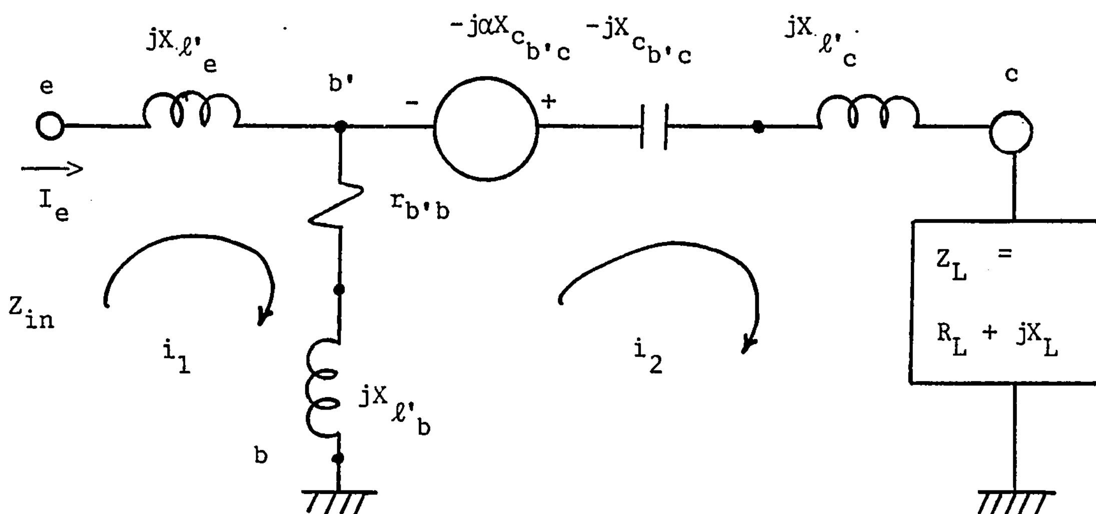


Figure 3. Converted modified Tee model

Let $I_e = 1A = I_{in}$

$$Z_{in} = E_s / I_{in} = E_s$$

$$E_s = j\omega(\ell'_e + \ell'_b) + r_{b'b} - (j\omega\ell'_b + r_{b'b})\, i_2$$

$$-j\alpha X_{C_{b'c}} = [j_\omega(\ell'_b + \ell'_c + \ell_L) - jX_{C_{b'c}} + r_{b'b} + R_L]\, i_2 - (jX_{\ell'b} + r_{b'b})$$

Assuming the collector to be conjugately matched,

$$-j\alpha X_{c_{b'c}} = (r_{b'b} + R_L)\, i_2 - (jX_{\ell'b} + r_{b'b})$$

results in

$$i_2 = \frac{-j\alpha X_{c_{b'c}} + jX_{\ell'_b} + r_{b'b}}{r_{b'b} + R_L} .$$

Substituting i_2,

$$E_s = Z_{in} = j\omega(\ell'_e + \ell'_b) + r_{b'b} - (j\omega\ell'_b + r_{b'b})\left(\frac{-j\alpha X_{c_{b'c}} + jX_{\ell'_b} + r_{b'b}}{r_{b'b} + R_L} \right).$$

$R_L > r_{b'b}$ allows the last term above to be ignored, resulting in

$$Z_{in} = j\omega(\ell'_e + \ell'_b) + r_{b'b}.$$

The output circuit of the unilateral equivalent circuit was developed in the same manner as the input circuit above. The complete unilateral equivalent circuit is represented in Figure 4.

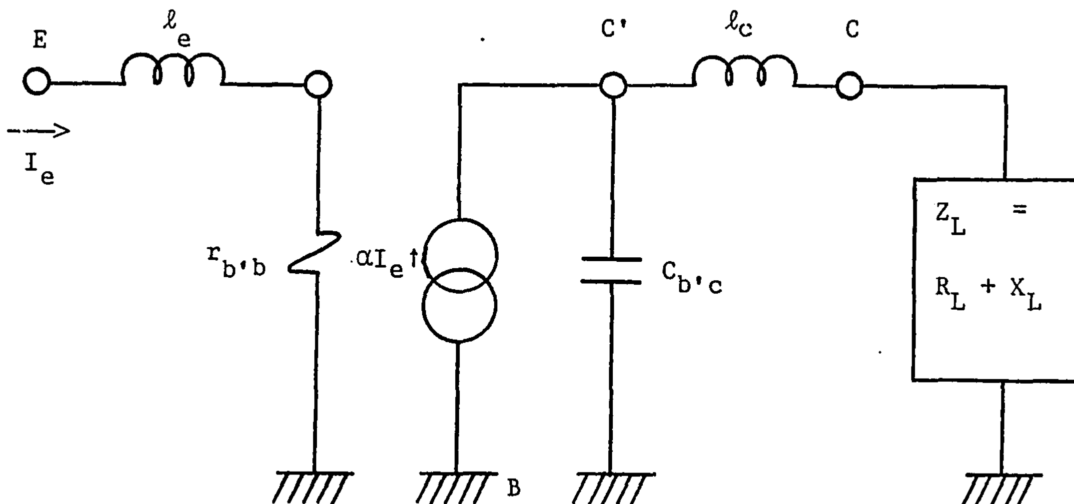


Figure 4. Unilateral equivalent circuit model

Conditions:

$R_L > r_{b'b}$

X_L provides the required conjugate reactance at the collector

$\ell_e = \ell'_e + \ell'_b$

This concludes the formal derivation of the unilateral equivalent circuit model [43] which is the basis of the model derivation to be employed within this dissertation. All further model development shall apply to the collector output portion of the model shown in Figure 5.

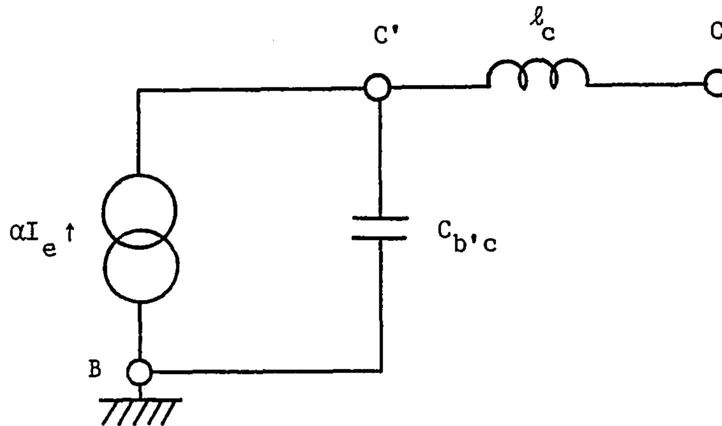


Figure 5. Basic collector output model

3.3.1. Basic model development

The basic model in Figure 5 as derived in Section 3.3 provides a very simple circuit description of the transistor during the active portion of the RF cycle.

The collector to base capacitance ($C_{b'c}$) in Figure 5 is the sum of two major capacitances. These capacitances are the package capacitance

which is the composite sum of all internal parasitic die and header capacitances and the junction depletion capacitance (C_t). The junction transistor (depletion) capacitance is dependent upon the collector-base voltage. The depletion capacitance may be defined [25] as:

$$C_t = \frac{K}{(V)^{1/n}}$$

where:

K = material constant.

V = sum of the junction barrier potential (V_B) and the reverse biased junction bias (-V) representing the voltage across the space-charge layer ($V = V_B - V$).

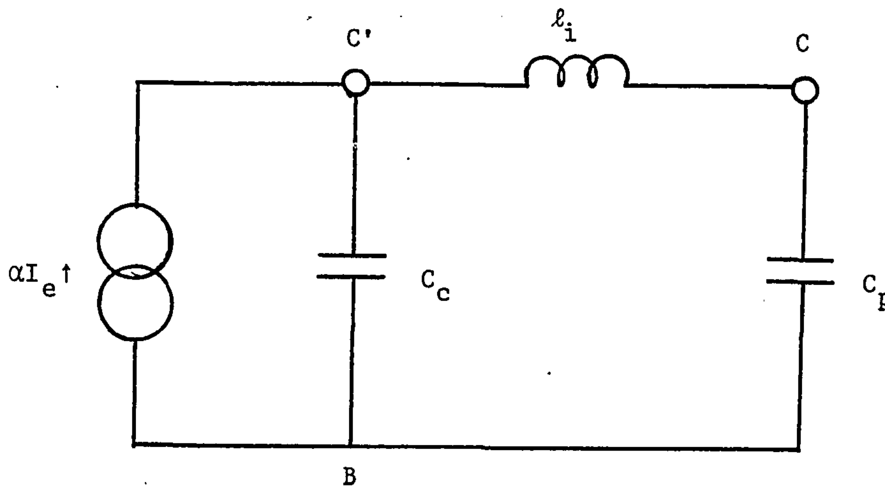
n = junction constant corresponding to the junction profile.
n = 2 (abrupt junction).
n = 3 (graded junction).

The relative capacitance values of the two contributing capacitive sources of $C_{b'c}$ are dependent upon the specific device. The package header capacitance (C_p) will generally have a value in the range of (0.6 to 1.6) pF. The larger values represent the largest packaged devices. The internal parasitics and die capacitances will vary, dependent upon the geometric design and the number of base cells within the device. The largest capacitive contribution is provided by the depletion capacitance corresponding to approximately two-thirds of the $C_{b'c}$ capacitance value [51, 59, 61].

The collector to base capacitance (C_{ob}) is measured at 1 MHz at a defined collector voltage. The measured C_{ob} capacitance represents the total sum of all the capacitance contributing to $C_{b'c}$ of the basic model

of Figure 5. Typically, the parasitic element values are not provided with device data sheets, but can usually be obtained from the manufacturer upon request.

The removal of the package capacitance (C_p) from the C_{ob} value provided by the manufacturer is defined as the collector to base capacitance value (C_c) in the finalized model configuration in Figure 6, such that $C_c = (C_{ob} - C_p)$.



ℓ_i = internal inductance ℓ_c from Figure 2.

C' = internal collector connection.

C = collector terminal external to the package.

Figure 6. Finalized collector output model including parasitic elements

The circuit configuration of Figure 6 represents the collector output model of a discrete transistor which has no internal output-matching elements within the discrete device package.

Devices utilizing internal matching elements may be incorporated

into the model by adding the internal matching elements in a similar manner as the parasitic elements in the model development.

3.4. Model Implementation

Microwave power amplifiers are normally operated without base bias. This is identified as a zero-biased power amplifier, which is frequently referred to as a zero bias Class-C amplifier. A true Class-C amplifier operation requires a base bias below cutoff to control the conduction angle (θ) to some value less than 180°. Frequently, input signal waveform shaping is used to further aid in the conduction angle reduction [31]. As a consequence of the zero-biased amplifier configuration when applied to sinewave amplification, the effective collector efficiency (η) is limited to that defined by either the Class-B single ended tuned output amplifier or the Class-C amplifier with a conduction angle $\theta = 180^o$.

Maximum power output efficiency for both Class-B and Class-C at $\theta = 180^o$ amplifiers is 78.5% for sinewave amplification [22, 70]. A proof of this for the Class-B case follows:

$$P_{in} = P_{dc} = V_{cc} I_{avg} = \frac{I_c V_{cc}}{\pi} \quad .$$

The average current (I_{dc}) for half the sinewave flowing through a resistive load is I_c/π. $I_c = 2V_o/R_L$, so, the output power (P_o) is:

$$P_o = \frac{V_o^2}{2R_L} = \frac{V_o}{4}\left(\frac{2V_o}{R_L}\right) = \frac{V_o I_c}{4} \quad .$$

Maximum output power (P_o) occurs when the peak output voltage (V_o) is equal to the dc collector supply bias (V_{cc}).

$$\eta = \frac{P_o}{P_{in}} = \frac{V_o I_c \pi}{4 V_{cc} I_c} = \frac{\pi V_o}{4V_{cc}} \leq \frac{\pi}{4} = 78.5\%.$$

For the Class-C case, the proof is slightly more complicated;

$$P_{in} = \frac{1}{2\pi} \int_{-\pi}^{\pi} V_{cc} \, i(t) \, d(\omega t) = \frac{2}{2\pi} \int_{0}^{\pi} V_{cc} \, i(t) \, d(\omega t)$$

where i(t) is the collector current. When i(t) is a portion of a sinewave within the conduction angle θ,

$$i(t) = I_o(\cos \omega t - \cos (\tfrac{\theta}{2})), \quad \frac{-\theta}{2} < \omega t < \frac{\theta}{2}$$

$$= 0 \quad , \text{ all other } \omega t.$$

Substituting and integrating results in

$$P_{in} = \frac{V_{cc} I_o}{\pi} \left[\sin \frac{\theta}{2} - \left(\frac{\theta}{2} \right) \cos \frac{\theta}{2} \right].$$

The power dissipation (P_d) of the device is

$$P_d = \frac{1}{2\pi} \int_{-\pi}^{\pi} (V_{cc} - V_{cc} \cos \omega t) \, i(t) \, d(\omega t)$$

$$P_o = P_{in} - P_d = \frac{V_{cc} I_c}{4\pi} (\theta - \sin \theta)$$

$$\eta_\theta = \frac{P_o}{P_{in}} = \frac{\theta - \sin \theta}{4 \sin \theta/2 - 2\theta \cos \theta/2}$$

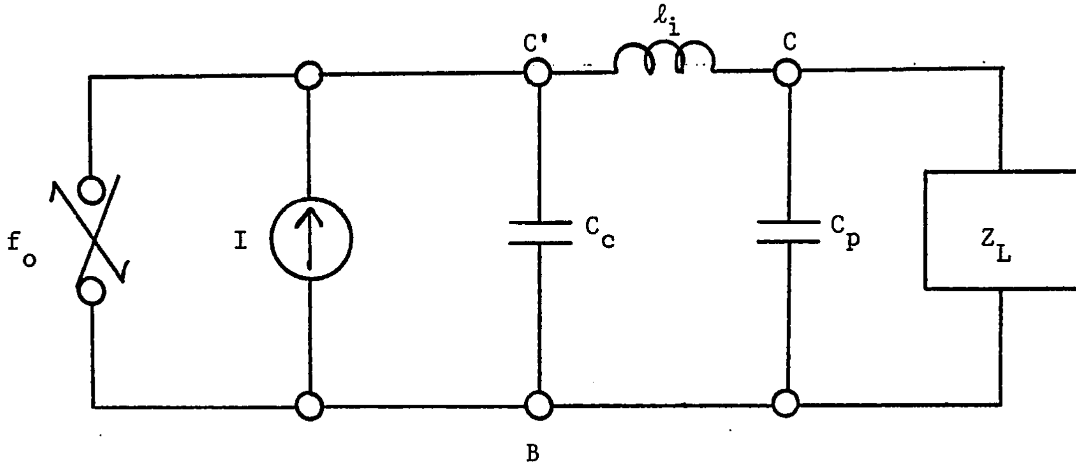
$$\eta_{(\pi)} = \frac{\pi - \sin(\pi)}{4 \sin (\pi/2) - 2\pi \cos (\pi/2)} = \frac{\pi}{4} = 78.5\%.$$

3.4.1. Transistor function

The functional assumptions used within the model implementation are outlined below.

When used in the design of a zero-biased microwave power amplifier driven by a symmetrically periodic 50% duty cycle signal current source, a transistor functions as a high speed switch. Also, when the amplifier is conjugately load matched and the input signal source power is increased to a sufficient level so as to produce the maximum output power, the switching efficiency of the transistor is maximized. The switching efficiency is increased by reducing the transistor switch transition time within the linear conduction region. An ideal transistor switch would appear to be either off with no current flow or current saturated in the on position. Both cases result in minimizing the power dissipation within the device during the switching period.

Based upon the transistor switch concept, the controlled current source in Figure 6 will be replaced by an ideal switch and a dc current source. This model change reflects the presumed fast switching speed ability of the transistor and includes the dc current source. The amplifier dc supply functions as a constant current source at the operating frequency. The result of these model modifications is represented in Figure 7 which includes a conjugately matched collector load.
The transistor amplifier collector output model in Figure 7 can be further simplified to the parallel configuration in Figure 8 using standard circuit transformations.



I = parallel switch shunted ideal current source.

Z_L = conjugately matched collector load $= R_L + jX_L$.

Figure 7. Transistor amplifier collector output model

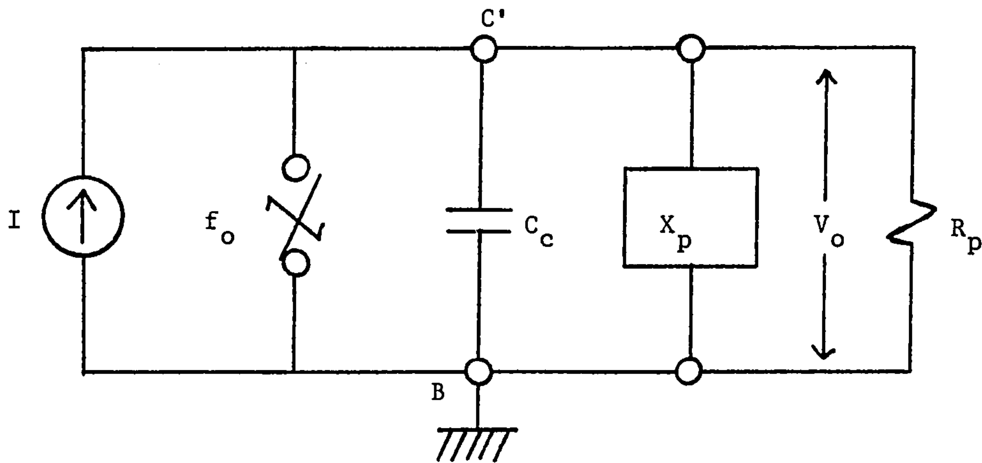


Figure 8. Final collector output model

Here:

X_p = the conjugate reactance equal to $|X_{c_c}|$ at the fundamental frequency (f_o).

R_p = the parallel resistive ohmic load.

For this model, the transistor switch in Figure 8 shall be assumed to be performing the following functions:

a) Provides an ideal switch shunted current source, which produces a periodic 50% duty cycle of period (τ) representative of the fundamental frequency (f_o). The switch also provides the high conductance condition realized during the transistor saturated conduction period.

b) Provides the effective capacitive reactance element (X_{c_c}) for resonance of the parallel modeled load impedance (R_p, X_p).

3.5. Model Application

Starting with the developed model configuration in Figure 8, the zero biased microwave power amplifier collector terminal output load impedance and performance efficiency (η) may be predicted, providing a very good first order design performance. Correlation of amplifier performance data to this transistor modeling procedure exhibits a very good agreement between predicted performance and measured performance.

The first step in a microwave power amplifier design is to select a transistor device which is frequency and power rated within the amplifier design requirements. The major parameters of immediate concern are power

output (P_o), collector voltage rating (V_{cc}), RF collector saturation voltage (V_{sat}), and collector-to-base capacitance (C_{ob}). The internal parasitic inductances and package capacitance are required for the discrete transistor in contrast with the internally matched newer generation of devices currently becoming popular for specialized applications. Internally matched devices require knowledge of the internal matching configuration and element values to allow circuit reduction to the model representation in Figure 8.

3.5.1. Definition of model values

The terms and definitions as defined below will be used:

Term	Definition
V_o	The amplitude of the sinusoidal output voltage.
P_o	The amplifier output power of the (CW) fundamental frequency (f_o).
V_{cc}	Collector bias supply voltage.
I_{dc}	The collector voltage bias supply current.
P_{in}	The dc supply power provided by the collector voltage bias supply, ($P_{in} = V_{cc}\ I_{dc}$).
P_d	The dissipation of lost power is represented as the difference between the P_{in} and P_o values ($P_d = P_o - P_{in}$). The power loss is usually assumed dissipated within the device. The dissipated power (P_d) is composed of two basic power loss elements: P_{d1} the nominal power dissipation of a Class-B amplifier operating at 78.5% efficiency, and the power loss of the device collector

to base output capacitance (C_c) identified as P_{d2} such that ($P_d = P_{d1} + P_{d2}$).

C_{ob} — The manufacturer supplied collector-to-base capacitance value.

C_p — The transistor package (header) capacitance value.

C_c — The collector-to-base value used in the model such that ($C_{ob} - C_p = C_c$).

R_p — The ohmic amplifier load.

ℓ_i — The internal series collector parasitic conductance.

V_{sat} — The RF saturation voltage is the result of a non-linear function of emitter current density and signal frequency [56]. $V_{sat} = kV_{cc}$, where typically $k < \frac{1}{4}$. Current transistor technology-developed devices which, when operated within their design parameters, exhibit maximum V_{sat} voltages between 1-3 volts. Manufacturers recommend using a first order approximation of (0.1) V_{cc} as a starting value for the V_{sat} voltage when V_{cc} is the rated maximum recommended value.

X_p — The conjugate reactance equal in magnitude to the reactance of C_c at the fundamental amplifier frequency (f_o), $|X'_p| = |X_{c_c}|$.

P_{d2} — Additional power dissipated through the transistor switch resulting from the collector output capacitance (C_c) during switch mode operation.

P_{d1} — Power dissipation of a Class-B amplifier operating at

78.5% efficiency.

Z_{cl} The collector output load impedance as viewed from the collector package terminal connection toward the load.

3.5.2. Model defined values

The model in Figure 8 represents the output portion of the power amplifier circuit. The overall configuration allows immediate calculation of values. Using the determined circuit values combined with the performance parameters desired, a complete circuit based on the model can be developed. The efficiency (η) and the required collector output terminal impedance (Z_{cl}) are easily calculated.

3.5.2.1. Output ohmic load resistance

The parallel resistance (R_p) is immediately determined from the model in Figure 8 as [71].

$$R_p = \frac{V_o^2}{2P_o} = \frac{(V_{cc} - V_{sat})^2}{2P_o} \tag{3.1}$$

The model assumptions establish the conditions of operation from which the output power (P_o) is maximized. Maximum real power transfer to the load can be realized only when the output voltage and current are in phase. This inphase relationship establishes the resonant condition of the output network. The amplitude of the output voltage (V_o) is assumed to be equivalent to the collector bias supply voltage (V_{cc}). The effect of the saturation voltage reduces the effective collector voltage to ($V_{cc} - V_{sat}$) resulting in Equation 3.1 above. The output voltage waves forms at R_p are

$$V_o(t) = V(1 - \sin \omega_o t)$$

and the output power is

$$P_o = \frac{V^2}{2R_p} \quad . \tag{3.2}$$

<u>3.5.2.2. Power dissipation</u> The power dissipation (P_d) is composed of two separate elements P_{d1} and P_{d2}. The first element, P_{d1}, represents the power lost (dissipated) relative to an assumed ideal Class-B amplifier. The maximum efficiency of a Class-B amplifier is 78.5%. Therefore, the power dissipation (P_{d1}) is $(1 - \frac{\pi}{4})P_{in}$. The second element, P_{d2}, results from the very high conductance of the transistor during the on-saturated-conduction portion of the transistor switching cycle. During the conduction period, the transistor switch appears as a near short circuit to ground for the energy stored in the collector-to-base capacitance (C_c). In addition to the energy which is dissipated within the device when assuming the ideal Class-B operation, this energy must be continuously dissipated and replaced each period under steady state operating conditions. For the above reason, $P_d = P_{d1} + P_{d2}$ represents the total power dissipation of the transistor switch as expressed by Equation 3.5 which will be derived below.

Let

$$W_c = \tfrac{1}{2}C_c V^2(1 - \sin \omega_o t)^2$$

be the energy stored in C_c at $t = 0$.

Expanding the above energy expression and integrating over the period (τ), the average energy over period (τ), $< W_c >$ is obtained as expressed below in Equation 3.3.

$$\frac{1}{\omega_o T} \int_0^{\omega_o T} [\tfrac{1}{2}C_c V^2 - C_c V^2 \sin\omega_o t + \tfrac{1}{2}C_c V^2 \sin^2\omega_o t] \, d\omega_o t$$

↑ average dc value (for $\tfrac{1}{2}C_c V^2$)

↑ zero average value (for $C_c V^2 \sin\omega_o t$)

↑ average ac component value (for $\tfrac{1}{2}C_c V^2 \sin^2\omega_o t$)

$$= \langle W_c \rangle = \tfrac{1}{2}C_c V^2 + \tfrac{1}{4}C_c V^2 \quad . \tag{3.3}$$

↑ capacitance energy loss term (for $\tfrac{1}{2}C_c V^2$)

↑ energy stored in the tuned circuit (for $\tfrac{1}{4}C_c V^2$)

The capacitance energy loss term (P_{d2}) is given as:

$$P_{d2} = \tfrac{1}{2}C_c V^2 f_o \quad . \tag{3.4}$$

The resulting power dissipation term (P_d) is:

$$P_d = P_{d1} + \tfrac{1}{2}C_c V^2 f_o \; . \tag{3.5}$$

3.5.2.3. Input power The input power (P_{in}) is defined as the product of the supply voltage (V_{cc}) and the supply dc average current (I_{dc}). The theoretical performance of a properly operating amplifier defines the input power (P_{in}) to be equal to the sum of the output power (P_o) and the dissipated power (P_d) as described below:

$$P_{in} = V_{cc} I_{dc} = P_o + P_d$$

$$= P_o + P_{d1} + P_{d2} \quad .$$

The maximum efficiency obtained from the assumed Class-B operating in sinusoidal amplification is 78.5%.

$$P_{in} = P_o + (1 - \tfrac{\pi}{4}) P_{in} + P_{d2}$$

where

$$P_{d1} = (1 - \frac{\pi}{4}) P_{in}$$

$$0.785 P_{in} = P_o + P_{d2}$$

$$P_{in} = \frac{P_o + P_{d2}}{0.785} = V_{cc} I_{dc} \quad (3.6)$$

$$P_{in} = \frac{V^2/2R_p + \frac{1}{2}C_c V^2 f_o}{0.785}$$

$$= 2V^2(1 + C_c R_p f_o)/\pi R_p \equiv V_{cc} I_{dc} \quad . \quad (3.7)$$

From Equations 3.2 and 3.5 respectively,

$$P_o = \frac{V^2}{2R_p}$$

and

$$P_{d2} = \frac{1}{2}C_c V^2 f_o \quad .$$

3.5.2.4. Collector conversion efficiency Amplifier efficiency is defined as the ratio of the power output (P_o) to the dc power input (P_{in}). The ratio for the Class-B ideal case is 0.785 or commonly referenced in percent as 0.785 x 100 = 78.5%. In practice, the actual efficiency will always be less than the ideal case.

$$\text{Efficiency} = \eta = \frac{P_o}{P_{in}} = \frac{P_o}{V_{cc} I_{dc}} \quad . \quad (3.8)$$

A very informative relationship is obtained by expanding the

efficiency Equation 3.8. This expansion is obtained by substituting Equation 3.2 and Equation 3.7 into Equation 3.8, resulting in the expanded efficiency Equation 3.9.

Let

$$\eta = \frac{P_o}{P_{in}} = \frac{V^2/2R_p}{2V^2(1 + C_cR_pf_o)/\pi R_p} = \frac{\pi}{4(1 + C_cR_pf_o)} \qquad (3.9)$$

where

$$R_p > 0.$$

The simplified expression of Equation 3.9 defines the amplifier efficiency. The relative contributing effects of the collector-to-base capacitance (C_c), the ohmic parallel equivalent load (R_p) and the fundamental frequency (f_o) are clearly described.

The efficiency expression is predicated upon the limits of the collector output model shown in Figure 8. The predicted efficiency is maximized at the maximum power output conditions which require the minimum R_p. The expected reduced efficiency at the higher fundamental output frequencies is supported by the basic low pass characteristics of the model in Figure 5. The capacitive loss term determined in Equation 3.4 predicts the reduced efficiency effects relative to the capacitance. The importance of a low value of collector capacitance is evident. From the model definition, it would appear that if the collector capacitance is ideally zero, the maximum efficiency of the Class-B amplifier would be achieved. The efficiency would in fact start to approach 78.5%, which is the limiting value.

3.6. Summary

The model is tested in Section 4. Measured amplifier performance data is compared with the model's predicted performance. The compared results show very good correlation between the model's predicted performance and the amplifier measured values.

It should be noted here that the model's success has been primarily based upon the relative magnitudes of the predicted performance to the measured performance.

4. TESTING OF THE COLLECTOR OUTPUT MODEL

4.1. Introduction

In this section, the model developed and defined in Section 3 will be used to provide the amplifier design parameters of a specific transistor. Amplifier performance measurements will be made and compared with the model defined design values to demonstrate potential accuracy of the model in practical applications.

Amplifier performance measurements will be obtained using four transistor samples. During each measurement, both the input and output loads will be impedance matched to the transistor. The measurements will be conducted at three different frequencies: 1.0, 1.1 and 1.2 gigahertz (GHz). The three different frequency measurements will be repeated for each of four different collector bias supply voltage (V_{cc}) 22, 24, 26, and 28 volts dc.

Each independent transistor measurement shall be conducted to reflect the transistor performance at maximum power output. In order to provide measurement consistency for comparison purposes, maximum power output is defined as the maximum output power of the fundamental frequency (f_o).

4.2. Measurement Test Fixture

The microwave test fixture identified in Figure 9 is specifically constructed to provide maximum design versatility. The variations of transistor package styles and internal configuration flexibilities present a broad range of mounting variations. The fixture employs a subassembly constructed design which provides for the interchange of

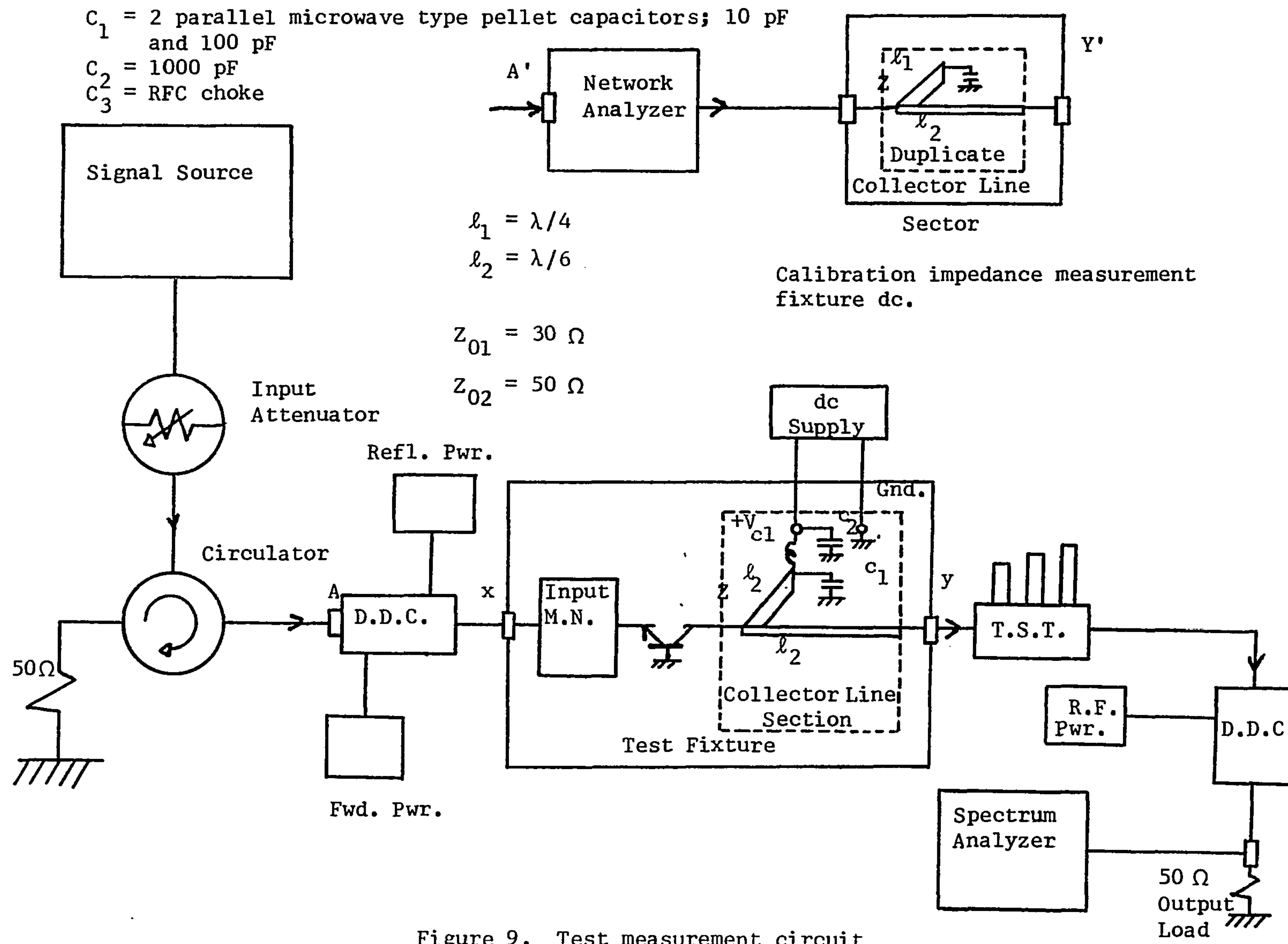


Figure 9. Test measurement circuit

the circuit base mounting platen assembly. This interchangeability permits complete amplifier input and output matching network designs to be integrated directly into the test fixture for test and evaluation during the design development.

The RF input and output connectors interfacing the test fixture are of the microstrip compression coaxial (SMA) type. The connectors are attached to the fixture on adjustable rail compression mounting posts which provide complete positioning location flexibility.

In addition to the above mechanical functions, the fixture must have provisions for the electrical connections between the transistor and the input and output matching networks. Also, it must provide a thermal heat sink for the test transistor. The thermal requirements demand the test fixture provide sufficient thermal mass to keep the transistor temperature relatively constant during the tuning process. The use of low-loss microstrip circuits combined with low-loss microwave lumped capacitors provides the electrically integrated interface.

4.3. Test Fixture Application

The test fixture for the transistor performance measurements which follow was specifically set up to include the use of a triple stub tuner to replace the discrete collector output matching network as shown in Figure 9. This alteration facilitated the use of the network analyzer for impedance measurements of the collector load. The triple stub tuner is disconnected at point Y as defined in Figure 9, then transferred and reconnected to Y' of the calibrated impedance measurement fixture. The reflection coefficient measurements of the transistor

collector load define the collector load impedance (Z_{cl}).

The collector impedance measurement fixture contains an identical duplicate of the collector line section used in the amplifier test fixture. These two duplicate line sections were pre-test calibrated to produce identical frequency characteristics over the range of test frequencies. Because of the use of duplicate collector line sections, all reflection coefficient measurements represent the transistor collector load impedance (Z_{cl}) presented to the transistor at Z as shown in Figure 9. The collector line section has incorporated within it an RF grounded quarter-wave ($\lambda_o/4$) line. The grounded quarter-wave line provides both the collector bias voltage supply isolation and a very low impedance path to ground for the second harmonic energy. The design frequency of 1.1 GHz was used for the collector line section which was found to be satisfactory for the required frequency excursion of (1.0 - 1.2) GHz.

The transistor drive was applied to the transistor through an input impedance matching network as shown in Figure 9. The input matching network assembly forms an integral part of the test fixture. The matching network is composed of a combination of distributed microstrip line sections and discrete capacitance. The basic circuit configuration represents a simple low-pass impedance transformation which exhibits sufficient band-pass to be easily tuned to provide a conjugately matched input over the required test frequency range.

4.4. MSC 81020 Transistor

The selected transistor type used for the following measurements was an MSC 81020. This transistor is representative of the current microwave device technology. Because of the broad range of acceptance for both military and industrial applications, the developmental maturity of this transistor is well-established. Due to the high volume usage of this device, major areas of uncertainty commonly associated with the initial release of newly designed transistors are removed. By design applications and use, transistor parameters, reliability and performance characteristics are well-known. For the above reasons this device has been chosen to be representative of a typical, good quality, discrete microwave transistor for the test measurements. The device rating nomenclature is as listed below.

<u>Maximum Ratings (typical)</u>

V_{cbo}	45 V
V_{cer}	45 V
C_{ob}	19 pF
Thermal resistance	5.5 ^{o}C/W
I_c (max)	6 A
P_{in} (max)	3 W
P_{out} (min)	20 W @ 1.0 GHz
	V_{cc} = 28 V
	P_{in} = 2 W

4.4.1. Transistor amplifier model

The transistor collector output model developed in Section 3 shall be used to predict the amplifier collector output design requirements and expected performance for the MSC 81020 device.

The transistor ratings and manufacturer supplied estimates of the parasitic element values and the RF saturation voltage (V_{sat}) provide the minimum required information necessary to construct the collector output model of the transistor as shown below.

Design Parameters

V_{cc} = 28 V

P_o = 20 W

C_{ob} = 19 pF

f_o = 1.0 GHz

C_p = (1.0 - 1.3)pF (1.1 pF used)

ℓ_i = (1.0 - 1.2)nH (1.1 nH used)

V_{sat} = (1.0 - 2.0)V (1.5 V used)

By using Equation 3.1, R_p is estimated to be:

$$R_p = \frac{(28 - 1.5)^2}{2(20)} = 17.6\ \Omega$$

The collector capacitance (C_c) is determined as

$$C_c = C_{ob} - C_p$$

$$C_c = (19.0 - 1.1) = 17.9\ \text{pF}.$$

The expected amplifier efficiency is calculated using Equation 3.9

for operation at 1.0 GHz as shown below.

$$\eta_{(1.0\ \text{GHz})} = \frac{\pi}{4(1 + (17.6)(17.9\text{x}10^{-12})(1.0\text{x}10^{9}))} \text{ X } 100 = 60\%.$$

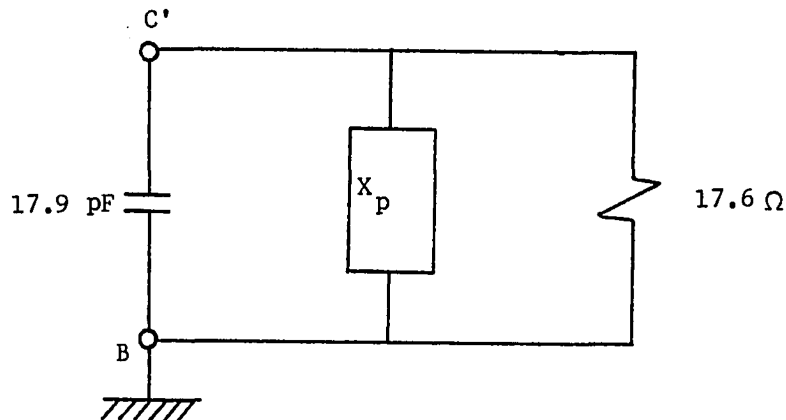
Using a supply voltage (V_{cc}) of 28 V_{dc}, the expected dc supply current is predicted using the calculated expected efficiency as shown below.

$$\frac{P_o}{\eta V_{cc}} = I_{dc} = \frac{20}{(0.6)(28)} = 1.19 \text{ A} \quad .$$

The power dissipation is also calculated to be

$$P_d = P_{in} - P_o \equiv (I_{dc})(V_{cc}) - 20 = 13.3 \text{ W} \quad .$$

The basic operational design parameters have been determined. The collector output model in Figure 10.



Operational parameters:

V_{cc} = 20 V $\quad P_o$ = 20 W $\quad I_{dc}$ = 1.19 A $\quad \eta$ = 60%

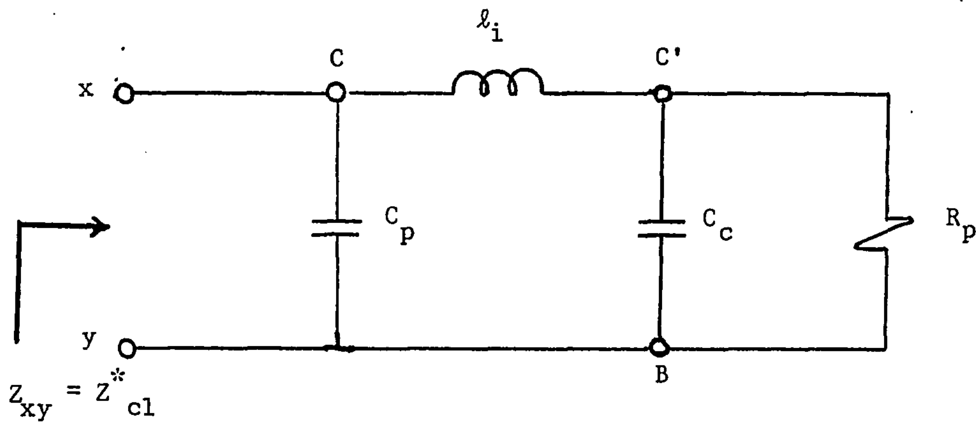
f_o = 1.0 GHz $\quad P_d$ = 13.3 W $\quad \left|X_p\right| = \left|\frac{1}{\omega_o C_c}\right|$

Figure 10. The design model

4.4.2. Using the parasitic element values

The design model shown in Figure 10 may be expanded to provide the collector load impedance (Z_{cl}) by using conventional linear circuit analysis methods. The output impedance (Z_{cl}) is ultimately needed to design the collector output matching network. The model developed in Section 3 describes the output impedance dependency upon the various amplifier operational parameters. This dependency together with the difficult, low impedance measurement limitations are the primary reasons why the typical output impedance values provided by the manufacturer are usually unrealizable for design purposes.

The collector output impedance for the model amplifier is calculated from the circuit configuration in Figure 11.



Z^* denotes conjugate value

Figure 11. Circuit model configuration for calculation of Z_{xy}

This calculation may be obtained by using any of the many available computerized linear network analysis programs (LNAP) or by simple independent calculations as described below.

The circuit configuration in Figure 11 is obtained by circuit conversion as illustrated in Figure 12.

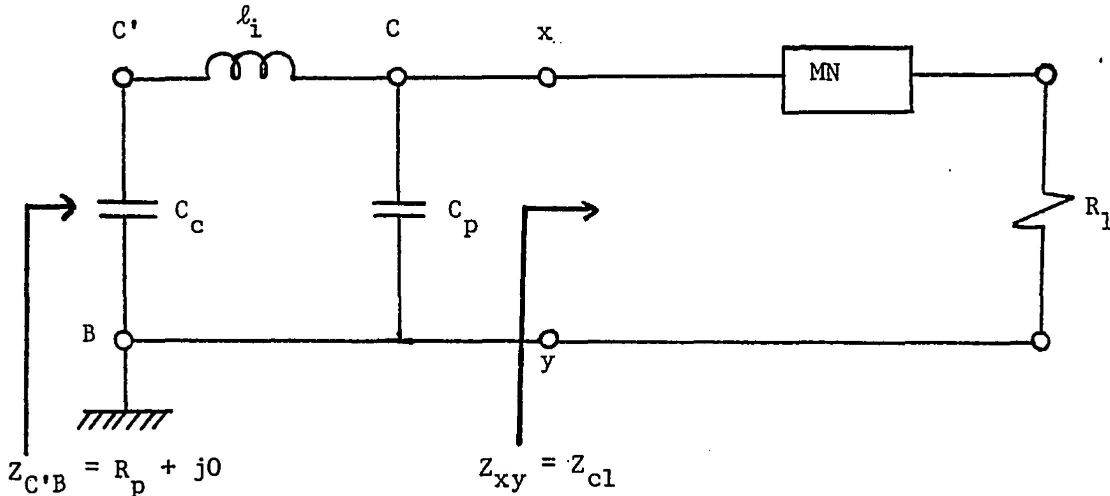


Figure 12. Expanded collector output including the output load network

The collector load impedance defined for the model in Figure 12 is $Z_{c'b} = R_p + j0$. The reactive part of the collector impedance (j0) is defined by either the conjugately matched reactance required in the model development or the resulting resonance realized at the fundamental frequency (f_o). To determine the collector output impedance (Z_{cl}) in Figure 12, the conjugate of the collector output impedance defined as $Z^*_{cl} = Z_{xy}$ is obtained by simple ac network analysis applied to the circuit in Figure 11 using the transistor design parameters listed in Section 4.4.1. The resultant collector terminal load impedance is

$Z_{cl} = 3.57 + j(0.26)$.

4.5. Test Procedure

The test measurements were conducted by using four MSC 81020 transistors, identified as T_A, T_B, T_C, and T_D. Tests were made at three discrete frequencies: 1.0, 1.1, and 1.2 GHz. Four different collector bias voltages were used at each frequency: 22, 24, 26, and 28 volts.

The amplifier input impedance was adjusted to provide the minimum input reflected power for each test.

The output power level was maximized for each test by adjusting the output load impedance using the triple stub tuner. At the conclusion of the amplifier tuning for each test, the input RF drive power was adjusted to provide 0.2 dB of output power compression. The power compression provides assurance that each of the test measurements represents the transistor operating under a similar loading and drive level relative to the other test parameters. The power compression characteristic is evidence that the transistor is entering into deep saturation. Continued increase in input drive power produces an insignificant increase in the power output. However, the collector bias supply current rises rapidly, indicating the increasingly higher power dissipation within the device. The resulting reduced efficiency and limited power output is characterized by the onset of the base-widening phenomenon [52] and increased V_{sat} due to the increased collector current [61].

At the conclusion of amplifier tuning adjustments, the collector terminal output load (Z_{cl}) was measured by using the network analyzer as previously described in Section 4.3 and illustrated in Figure 9.

The above procedure was repeated for each test condition, using each of the four test transistors; T_A, T_B, T_C, and T_D.

4.6. Test Data

The outlined tests were performed and the measurements are recorded in Tables 1, 2, and 3.

The transistor V_{sat} voltage was observed under operating conditions by using a sampling oscilloscope. The manufacturer's recommended value of 1.5 V was observed to be too low. The test effective V_{sat} value was measured and determined to be 1.75 V, which was used in all further computations.

Using the recorded data from Tables 1, 2, and 3, and utilizing the three different approaches tabulated in Table 4, the amplifier dc to RF conversion efficiency was evaluated and compared. The first approach was the calculation of the true measured efficiency using Equation 3.8. This is the η (measured) value found in Table 4.

The second, alternate, approach is the calculated efficiency using Equation 3.9. The value of the collector to base capacitance (C_c) was determined as the average value from the 48 test measurements. The average C_c value used was 18.67 pF. The average parallel resistive load (R_p) was determined for each different test group. Using both C_c and R_p, the η(calculated) values were then computed.

The final approach defines collector efficiency relative to the design model depicted in Figure 8, and is identified as η (model). The required model element values used are the average value calculated above for C_c and the R_p values defined by Equation 3.1. The average power output of each of the 12 different test groups is used in the calculation of R_p.

Table 1. Amplifier performance data

Device	P_i W	P_o W	I_{dc} A	ρ $\lvert\rho\rvert$	ρ $\angle$
	$V_c = 28\ V_{dc}$		$f_o = 1.0$ GHz		
T_A	2.20	21.5	1.28	0.86	-179.5
T_B	2.15	22.0	1.29	0.88	-179.5
T_C	2.40	22.8	1.32	0.87	-180.0
T_D	2.20	21.8	1.30	0.87	-179.0
	$V_c = 26\ V_{dc}$		$f_o = 1.0$ GHz		
T_A	2.13	19.0	1.20	0.86	-179.4
T_B	2.00	18.8	1.18	0.87	-179.0
T_C	2.25	19.2	1.19	0.86	-179.2
T_D	2.15	19.2	1.22	0.88	-178.3
	$V_c = 24\ V_{dc}$		$f_o = 1.0$ GHz		
T_A	2.50	16.9	1.14	0.85	-179.1
T_B	2.32	16.4	1.10	0.86	-179.0
T_C	2.80	17.2	1.16	0.86	-178.7
T_D	2.63	17.0	1.16	0.86	-179.4
	$V_c = 22\ V_{dc}$		$f_o = 1.0$ GHz		
T_A	2.30	14.2	1.05	0.85	-179.0
T_B	2.29	14.8	1.07	0.85	-178.7
T_C	2.56	15.1	1.10	0.85	-178.2
T_D	2.50	14.1	1.04	0.85	-179.0

Table 2. Amplifier performance data

Device	P_i W	P_o W	I_{dc} A	ρ $\|\rho\|$	ρ ∠
	V_c = 28 V_{dc}			f_o = 1.1 GHz	
T_A	2.10	19.2	1.17	0.89	-176.9
T_B	2.40	20.1	1.21	0.88	-177.0
T_C	2.50	20.4	1.21	0.89	-176.9
T_D	2.00	19.7	1.21	0.88	-177.0
	V_c = 26 V_{dc}			f_o = 1.1 GHz	
T_A	2.44	17.3	1.13	0.88	-177.3
T_B	2.27	16.8	1.08	0.88	-176.7
T_C	2.60	17.1	1.09	0.88	-176.9
T_D	2.20	17.4	1.13	0.88	-177.1
	V_c = 24 V_{dc}			f_o = 1.1 GHz	
T_A	2.55	15.7	1.10	0.88	-177.4
T_B	2.35	15.9	1.09	0.87	-176.5
T_C	2.75	16.2	1.12	0.87	-176.7
T_D	2.80	16.1	1.11	0.87	-177.0
	V_c = 22 V_{dc}			f_o = 1.1 GHz	
T_A	2.24	13.2	0.99	0.87	-177.0
T_B	2.31	13.9	1.03	0.87	-176.1
T_C	2.63	13.8	1.03	0.87	-176.6
T_D	2.88	14.1	1.05	0.86	-176.6

Table 3. Amplifier performance data

	V_c = 28 V_{dc}			f_o = 1.2 GHz	
Device	P_i W	P_o W	I_{dc} A	ρ $\lvert\rho\rvert$	$\angle$
T_A	2.22	18.9	1.18	0.90	-174.6
T_B	2.47	19.2	1.22	0.91	-173.8
T_C	2.33	18.5	1.12	0.90	-174.1
T_D	2.15	17.9	1.10	0.90	-175.0
	V_c = 26 V_{dc}			f_o = 1.2 GHz	
T_A	2.62	16.9	1.13	0.89	-174.5
T_B	2.26	16.4	1.10	0.90	-174.5
T_C	2.80	16.5	1.09	0.89	-174.9
T_D	2.20	16.3	1.11	0.90	-174.4
	V_c = 24 V_{dc}			f_o = 1.2 GHz	
T_A	2.69	15.1	1.08	0.89	-174.5
T_B	2.74	14.7	1.04	0.90	-174.3
T_C	3.00	15.5	1.12	0.90	-174.6
T_D	2.55	15.0	1.11	0.90	-174.5
	V_c = 22 V_{dc}			f_o = 1.2 GHz	
T_A	2.55	12.2	0.94	0.88	-174.5
T_B	2.32	11.9	0.92	0.89	-174.0
T_C	2.45	11.7	0.91	0.88	-174.4
T_D	2.60	12.5	0.99	0.89	-174.5

Table 4. dc to RF conversion efficiency (η)

V_c V	η (measured) %	η (calculated) %	η (model) %
f_o = 1.0 GHz, V_{sat} = 1.75 V_{dc}, C_c = 18.7 pF			
28	60.6	60.8	60.7
26	61.2	61.2	61.0
24	61.7	61.7	61.6
22	62.3	62.5	62.2
f_o = 1.1 GHz, V_{sat} = 1.75 V_{dc}, C_c = 18.7 pF			
28	59.1	59.2	57.9
26	59.5	59.5	58.1
24	60.2	60.2	59.6
22	60.9	61.0	60.1
f_o = 1.2 GHz, V_{sat} = 1.75 V_{dc}, C_c = 18.7 pF			
28	57.1	57.5	55.5
26	57.7	58.2	56.1
24	58.3	57.9	57.4
22	58.9	59.3	57.0

Table 5. Parallel resistive output load (R_p)

V_c V	P_o (measured) W	R_p (measured) Ω	R_p (model) Ω
f_o = 1 GHz, C_c = 18.7 pF, V_{sat} = 1.75 V_{dc}			
28	22	15.6	15.7
26	19.1	15.1	15.4
24	16.9	14.6	14.7
22	14.6	13.7	14.0
f_o = 1.1 GHz, C_c = 18.7 pF, V_{sat} = 1.75 V_{dc}			
28	19.9	15.9	17.3
26	17.2	15.6	17.1
24	16.0	14.8	15.5
22	13.8	14.0	14.9
f_o = 1.2 GHz, C_c = 18.7 pF, V_{sat} = 1.75 V_{dc}			
28	18.6	16.3	18.5
26	16.5	15.6	17.8
24	15.1	15.9	16.4
22	12.2	14.5	16.8

Both the measured and model predicted R_p values are tabulated in Table 5 for comparative evaluation.

4.6.1. Model effectiveness at intermediate power output levels

The collector output model effectiveness has been evaluated relative to the transistor operational performance defined parameters. However, all tests have been restricted to describe the transistor performance only during operation at maximum output power. To evaluate the collector output model's use at other than maximum output power condition, the following tests were performed.

Tests at intermediate output power levels of 15, 13, and 11 watts were conducted. A collector bias voltage of 26 V_{dc} and fundamental frequency (f_o) of 1.1 GHz was used for the tests. The previously defined collector to base capacitance (C_c) of 18.7 pF was used to produce the collector output model predicted efficiency and R_p values in Table 6.

Table 6. Modeled intermediate output data

P_o W	R_p Ω	η %
11	22.7	51.0
13	22.6	54.0
15	19.6	55.7

f_o = 1.1 GHz

V_{cc} = 26 V_{dc}

C_c = 18.7 pF

The previously described measurement procedure in 4.5 was repeated with the following exceptions: the load matching adjustments were made to produce the measured data values, representing as closely as possible device characteristics, at the power output levels of 11, 13, and 15 watts. Only one device was used for these measurements. The measured test data are listed in Table. 7.

Table 7. Intermediate output power data

V_{cc} = 26 V_{dc} f_o = 1.1 GHz

measured							model		
P_o	I_{dc}	η	ρ		R_p	Cc	R_p	C_c	η
W	A	%	$\lvert\rho\rvert$	$\angle$	Ω	Pf	Ω	pF	%
11.2	0.86	50.1	0.92	-178.5	25.3	19.2	26.3	18.7	51.0
13.3	0.95	53.8	0.91	-178.2	22.1	19.1	22.1	18.7	54.0
14.8	1.02	56.0	0.89	-178.2	18.8	18.1	19.9	18.7	55.7

4.7. Measured Performance vs. the Collector Output Model

The dc to RF conversion efficiency (η) model predicted values defined by Equation 3.9 are very well-supported by the measured efficiency. This very close correlation between the measured and model defined values over the test range of frequency and collector voltage supports the interrelated dependencies described in Section 3.5.2.4 and defined in Equation 3.9.

The model derived R_p values and the performance defined values of R_p shown in Table 5 are in relatively close agreement at the lower frequency. The somewhat larger disagreement between the measured and

model-defined values of R_p at higher frequencies is supported by Krishna et al. [56] and Kirk [52]. The V_{sat} is both frequency and collector current density related. This relationship places a definite limitation upon the model use relative to the accuracy of the V_{sat} approximation used.

The model predicted performance disclosed excellent agreement at the intermediate output power levels as shown in Table 7. The close agreement reflects the lower collector current density experienced at the reduced output power level. Because of the reduced collector current the actual V_{sat} voltage did not increase beyond the estimated value.

5. SUMMARY, CONCLUSIONS AND FUTURE RESEARCH WORK

5.1. Summary and Conclusions

Large-signal microwave amplifier design is considerably more complicated than small-signal design. Small-signal amplifiers are generally designed to provide a specified gain over a defined bandwidth, relative to the design frequency. While well-defined stability boundaries are assured, input and output matching circuits can be mutually varied to meet an acceptable gain in small-signal design. In large-signal designs, the output-matching circuit must principally satisfy good collector efficiency and maximum saturated output power with good stability over the operating frequency range. While the output match also affects power gain, this factor is usually in conflict with the principal objective of saturated output power. Consequently, power gain often must be sacrificed from 1 to 2 dB from the maximum usable value. The input-matching circuit design is principally concerned with power-gain conservation and gain flatness. The design of the input circuit has no relationship to the saturated output power or collector efficiency.

Complete equivalent-circuit representations based on the scattering matrix, which account for forward and reverse power flows, are not available with large-signal microwave power amplifiers. Similarly transistor characterizations, that would serve large-signal objectives as effectively as the S-parameter characterization serves the small Class-A design, are not widely available. Where complete large-signal characterization has been undertaken, a large number of painstaking measurements

have been necessary. Even if complete S-parameter characterization were available, a new dilemma would present itself. While S-parameter characterization is excellent for assuring stability and level power gain in broadband designs, there are no significant means for S-parameter consideration of the two vital large-signal design factors: saturated power output and collector efficiency. These two factors are a function of the collector loadline impedance. S-parameter characterization would only permit relating the loadline to the output impedance of the transistor in terms of power gain and stability of the amplifiers. It does not provide characterization information necessary for assuring some objective minimum output power and/or collector efficiency in the design.

Transistor manufacturers offer some collector loading information for power transistors on transistor data sheets. These impedance data are given for rated output power over the normal frequency range of application for the particular device. There are several vague points in such data.

1. At what point on the collector lead is such data referenced?
2. When the real component of impedance is low, one is concerned that the losses present in the tuning stubs or other matching elements may be obscuring the measured impedance data.
3. How do the specified impedance values vary relative to changes in output power levels and bias supply voltages?
4. What are the deviation limits and associated effects allowed relative to the specified impedance data?

This dissertation has focused on this major design need.

A systematic approach to the characterization and design of the microwave transistor power amplifier has been developed. The technique provides accurate and rapid first order design data which can efficiently provide optimal designs when incorporated with CAD programs.

5.2. Improved Power Amplifier Characterizations

The large-signal transistor design model developed in Section 3 is based upon a few simple calculations and estimates of the internal parasitic elements which are determined by the package geometries and power levels.

There are two primary uses for the model. First, with very limited RF information, it will give a good, first-cut estimation of the transistor's output impedance. Secondly, if the collector output impedance characterization exists for one collector bias voltage, frequency and power output level, a very good estimate can be made of the impedance at a different voltage, power and/or frequency by an analysis of the model.

Additional operational parameter estimates may be derived utilizing the efficiency parameter. The derivation of Equation 3.9 defines the efficiency (η) parameters. This derivation clarifies the typically low RF to dc conversion efficiencies experienced in large-signal power amplifier designs.

A very important consideration in selecting a transistor for use in the design of a microwave power amplifier is the parasitic element values. Of particular importance is collector-to-base capacitance which should be as small as possible.

5.3. Future Research

This dissertation describes a successful approach to microwave power amplifier design. However, the success is dependent upon the model defined limitations and approximations described in Section 3.

One of the primary constraints of this modeling technique is the RF saturation voltage (V_{sat}) value. More work remains to be done to develop either a measurement technique or an analytical approach to better define the V_{sat} value.

Bandwidth design limitations relative to the model defined output impedance remain to be investigated. For broadband designs there are two available parameters for design control of bandwidth. These are the R_p value and the resultant combined reactance (X'_p) which represents the parallel reactance of X_{c_c} and X_p of the model. These represent the design constraints for the output matching network. They can be described in terms of an admittance at C' the internal collector node in Figure 8. This admittance is defined as $Y_{c'b} = 1/Z_{c'b}$; which is comprised of a conductance G and susceptance B. It is convenient to view this admittance as comprised of a parallel combination of a resistance $R_p = 1/G$ and a reactance $X'_p = 1/B$. The parallel resistance R_p is the resistive load which relates to the power output level desired principally as a function of the collector dc supply bias voltage V_{cc}.

At power levels below rated levels, R_p varies approximately inversely with the power output. Therefore, to assure near-constant saturated power output levels, R_p must vary inversely with frequency. These relationships are expressed mathematically by Equation 3.9. A reasonable load-line design approach is to maintain R_p at a fixed nominal

value over the operating bandwidth.

Transistor conversion efficiency (η) is optimal when the C_c is tuned out completely producing a purely resistive load R_p. However, this optimal condition is only attainable at one or more specific frequencies within a design bandwidth and is physically impossible to maintain continuously over a design bandwidth frequency range. The magnitude of X'_p permissible deviations which will provide good performance (high efficiency and output power) will be of extreme value in broadband designs. It should also be noted that both the reactive deviations and the load-line R_p variances may be combined to provide broadband design freedom.

5.3.1. High efficiency

High efficiency techniques which presently are not adaptable because of the constraints imposed by the parasitic elements in the current bipolar devices which may be alleviated by special transistor package designs and internal parallel shunt inductors. This is an area which presents significant opportunities worthy of investigation.

5.4. Summarization

Beyond the major accomplishments, the amplifier design technique and model development, three very significant facts have become apparent. First, there is an extreme need for improved high frequency measurement instrumentation to deal with the high frequency microwave design. Secondly, extremely high costs are incurred in conducting research in microwave areas. Lastly, there exists a rapidly growing need for microwave power amplification. Rapid expansion and growth in the microwave

spectrum is placing a growing demand for higher power and frequency performance.

6. REFERENCES

1. Hines, M. E. "Special Issue on Solid-State Microwave Power Amplifiers." IEEE Trans. Microwave Theory and Techniques MTT-21 (11) (Nov. 1973):657-659.

2. Locke, J. F. and G. Hodowanec. "Recent Developments in Microwave Transistors and Circuits." MSN 3 (6) (Oct./Nov. 1973):42-50.

3. Sparkes, J. J. "The First Decade of Transistor Development: A Personal View." Radio and Electronic Eng. 43 (1973):3.

4. Davies, R. T. "Microwave Power on the Rise." MicroWaves 13 (4) (April 1974):9.

5. Balshem, H. and T. Marks. "Solid State Power Amplifiers for Airborne DME Applications." MSN 5 (April/May, 1975):17-23.

6. Wheeler, C. A. and S. M. Livingston. "A Solid-State Amplifier for Satellite Communications." Microwave J. 18 (7) (1975):52-55.

7. Kaye, D. N. "RF and Microwave Series in Rising in Power and Declining in Noise." Electronic Design 81 (9) (Sept. 1, 1975): 34-36.

8. Grace, M. I. "Review of Microwave Amplifiers." Microwave J. 18 (11) (Nov. 1975):27-32.

9. Naragan, W. Y. "Medium Power GaAs MESFETS." Microwave J. 19 (2) (Feb. 1976):47-51.

10. Barrera, J. S. "Microwave Transistor Review Part 1." Microwave J. 19 (2) (Feb. 1976):28-31.

11. Poole, W. E. "Microwave Transistor Review Part 2." Microwave J. 19 (2) (Feb. 1976):31-36.

12. Pitzalis, Jr., O. "Status of Power Transistors Bipolar and Field Effect." Microwave J. 20 (2) (Feb. 1977):30-61.

13. Yates, W. "RF Transistors Target Low Noise, High Gain and Power." Electronics Prod. Mag. 23 (9) (1980):31-33.

14. Belohoubek, E. F. "Advanced Microwave Circuits." IEEE Spectrum 18 (2) (1981):44-47.

15. Holmquist, J. "Bipolars Ready for S-Band Radar." MSN 11 (7) (1981):100-103.

16. Milnes, A. G. "Semiconductor Devices Integrated Electronics." New York: Van Nostrand Reinhold Company, 1980.

17. Everitt, W. L. "Optimum Operating Conditions for Class C Amplifiers." Proc. IRE 22 (Feb. 1934):152-176.

18. Terman, F. E. and J. H. Ferns. "The Calculations of Class C Amplifier and Harmonic Generator Performance of Screen-Grid and Similar Tubes." Proc. IRE 22 (March 1934):359-373.

19. Everitt, W. L. "Optimum Operating Conditions for Class B Radio-Frequency Amplifiers." Proc. IRE 24 (Feb. 1936):305-315.

20. Terman, F. E. and W. C. Roake. "Calculations and Design of Class C Amplifiers." Proc. IRE 24 (April 1936):620-632.

21. Comer, D. T. "Large Signal Transistor Circuits." New York: Prentice Hall, 1967.

22. Krauss, H. L., C. W. Bostian and F. H. Raab. "Solid State Radio Engineering." New York: John Wiley & Sons, Inc., 1980.

23. Leighton, W. H., R. J. Chaffin and J. G. Webb. "RF Amplifier Design and Large-Signal S-Parameters." IEEE Trans. Microwave Theory and Techniques MTT-21 (Dec. 1973):809-814.

24. Belouhoubek, E. F. "Wideband Microwave Transistor Power Amplifiers." IEEE J. Solid State Circ. SC4-4 (Dec. 1969):360-367.

25. Bailey, R. L. "Large-Signal Non-Linear Analysis of a High-Power High-Frequency Junction Transistor." IEEE Trans. Electron Devices ED-17 (2) (Feb. 1970):108-119.

26. Harrison, R. G. "Non-Linear Theory of Class C Transistor Amplifiers and Frequency Multipliers." IEEE J. Solid State Circ. SC-4 (June 1969):178-179.

27. Johnston, R. H. and A. R. Buothroyu. "High-Frequency Transistor Frequency Multipliers and Power Amplifiers." IEEE J. Solid State Circ. SC-7 (1) (Feb. 1972):81-89.

28. Mulder. J. "On the Design of Transistor RF Power Amplifiers." Electron. Appl. 27 (1966):155-171.

29. O'Reilly, W. P. "Transmitter Power Amplifier Design, Part 1." Wireless World 81 (Sept. 1975):417-422.

30. O'Reilly, W. P. "Transmitter Power Amplifier Design II." Wireless World 81 (Oct. 1975):479-782.

31. Scott, T. M. "Tuned Power Amplifiers." IEEE Trans. Circ. Theory CT-11 (1964):358-389.

32. Slatter, J. A. G. "An Approach to the Design of Transistor Tuned Power Amplifiers." IEEE Trans. Circ. Theory CT-12 (June 1965):206-211.

33. Snider, D. M. "A Theoretical Analysis and Experimental Confirmation of the Optimally Loaded and Overdriven RF Power Amplifier." IEEE Trans. Electron Devices ED-14 (12) (Dec. 1967):851-857.

34. Ebers, J. J. and J. L. Moll. "Large-Signal Behavior of Function Transistors." Proc. IRE 42 (Dec. 1954):1761-1772.

35. Houselander, L. S., H. Y. Chow and R. Spence. "Transistor Characterization by Effective Large-Signal Two-Part Parameters." IEEE J. Solid State Circ. SC-5 (1970):77-79.

36. Kotzebue, K. L. "Microwave-Transistor Power-Amplifier Design by Large-Signal of Parameters." Electronics Letters 11 (11) (May 29, 1975):240-241.

37. Kotzebue, K. L. "A New Technique for the Direct Measurement of Y-Parameters at Microwave Frequencies." IEEE Trans. on Instrumentation and Measurement M-26 (2) (June 1977):119-123.

38. Belouhoubek. "Hybrid Integrated 10-watt CW Broadband Power Source at S-Band." IEEE J. Solid State Circ. SC-4 (Dec. 1969):360-367.

39. Takayama, Y. "A New Load-Pull Characterization Method for Microwave Power Transistors." Inter. Microwave Symposium, Digest of Technical Papers, IEEE MTT-S (1971):218-220.

40. Presser, A. and E. Belohoubek. "1-2 GHz High-Power Linear Transistor Amplifier." RCA Rev. 33 (Dec. 1972):737-751.

41. Cusak, J. M. "Automated Load Contour Mapping for Microwave Power Transistors." IEEE Trans. Microwave Theory and Techniques MTT-22 (12) (Dec. 1974):1146-1152.

42. Lange, J. "A Survey of the Present State of Microwave Transistor Modeling and Simulation as Applied to Circuit Design." IEEE Trans. Electron Devices ED-18 (12) (Dec. 1971):1168-1174.

43. Linvill, J. G. "Models of Transistors and Diodes." New York: McGraw Book Company, 1963.

44. Sparkes, J. J. and R. Beaufay. "The Function Transistor as a Change Controlled Device." Proc. IRE 45 (1957):1740.

45. Peden, R. D. "Charge-Driven HF Transistor-Tuned Power Amplifier." IEEE J. Solid State Circ. SC-5 (2) (April 1970):55-63.

46. Gummel, H. K. and H. C. Poon. "An Integral Charge Control Model of Bipolar Transistors." Bell System Tech. J. 49 (1970):826.

47. Getreu, I. "A New Series, Modeling the Bipolar Transistor." Electronics 47 (Nov. 14, 1974):137.

48. Pritchard, R. L. "Transistor Internal Parameters for Small-Signal Representation." Proc. IRE 49 (1961):725.

49. Shackle, P. W. "An Experimental Study of Distributed Effects in a Microwave Bipolar Transistor." IEEE Trans. Electron Devices ED-21 (1874):32.

50. Krunquist, R. L. "Determination of a Microwave Transistor Model Based on an Experimental Study of its Internal Structure." Solid-State Electronics 18 (1978):949.

51. Wahl, A. J. "Distributed Theory for Microwave Bipolar Transistors." IEEE Trans. Electron. Devices ED-21 (1974):40.

52. Kirk, Jr., C. T. "A Theory of Transistor Cutoff Frequency (f_T) Fallout at High Current Densities." IRE Trans. Electron Devices ED-9 (1962):164.

53. Kumar, R. and L. P. Hunter. "Collector Capacitance and High-Level Injection Effects in Bipolar Transmittors." IEEE Trans. Electron Devices ED-22 (1975):51.

54. Rey, G. F. Dupuy, and J. P. Bailbe. "A United Approach to the Base Widening Mechanisms in Bipolar Transistors." Solid-State Electronics 18 (1975):863.

55. Collins, T. W. "Collector Capacitance Versus Collector Current for a Double-Diffused Transistor." Proc. IEEE 57 (1969):840.

56. Krishna, S., P. J. Kannan, and W. Doesschate, Jr. "Some Limitations of the Power Output Capability of VHF Transistors." IEEE Trans. on Electron Devices, ED-15 (11) (November 1968): 855-860.

57. Cooke, H. F. "Microwave Transistors: Theory and Design." Proc. IEEE 57 (Aug. 1971):1163-1180.

58. Benjamin, J. A. "New Design Concepts for Microwaves Power Transistor." Microwave J. 15 (10) (1972):39-64.

59. Johnson, E. O. "Physical Limitation on Frequency and Power Parameters of Transistors." RCA Rev. 26 (June 1965):163.

60. Poole, W. E. "Microwave Transistor Review - Part 2 - Microwave Bipolar Transistors." Microwave J. 19 (2) (1976):31.

61. Tatum, J. G. "Microwave Transistor Parameter Trade-Offs in Circuit Design, Part 3." MicroWaves 6 (11) (1967):44-53.

62. Conn, D. R. and R. H. Mitchell. "Small-Signal Characteristics of Lateral Transistors." Int. J. Electronics 34(1973):655.

63. Carson, R. S. "High-Frequency Amplifiers." New York: John Wiley & Sons, Inc., 1975.

64. Graham, Jr., E. P. G. W. Guyn and R. J. Chaffin. "Device Physics Simulation." Microwave J. 18 (2) (1975):37.

65. Harrison, R. G. "Computer Simulation of a Microwave Power Transistor." IEEE Solid-State Circuits SC-6 (1971):226.

66. Heimeier, H. H. "A Two-Dimensional Numerical Analysis of a Silicon n-p-n Transistor." IEEE Trans. Electron Devices ED-20 (1973):708.

67. Seltz, D. S. and I. Kidron. "A Two-Dimensional Model for the Lateral p-n-p Transistor." IEEE Trans. Electron Devices ED-21 (1974):587.

68. Slotboum, J. W. "Computer-Aided Two-Dimensional Analysis of Bipolar Transistors." IEEE Trans. Electron Devices ED-20 (1973):169.

69. Johnson, J. "Solid Circuits." San Carlos, California: Communications Transistor Company, 1973.

70. Ha, T. T. "Solid State Microwave Amplifier Design." New York: John Wiley & Sons, Inc., 1981.

71. RCA Designer's Handbook. "Solid-State Power Circuits. Somerville, New Jersey: Technical Series SP-52 (1971).